IN THE SPECIFICATION:

Please amend paragraph **[0002]** as follows:

[0002] This application is related to: an application having Serial No. 08/591,238, filed January 17, 1996, entitled "METHOD AND APPARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED ~~CIRCUIT",~~ CIRCUIT," abandoned in favor of a ~~continuation-in-part~~ continuation-in-part application filed February 27, 1998, having Serial No. 09/032,417, and entitled "METHOD AND APPARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED ~~CIRCUIT",~~ CIRCUIT," now U.S. Patent 6,194,738, issued February 27, 2001; an application having Serial No. 08/664,109, filed June 13, 1996, entitled "A STRUCTURE AND A METHOD FOR STORING INFORMATION IN A SEMICONDUCTOR ~~DEVICE",~~ DEVICE," now U.S. Patent 5,895,962, issued April 20, 1999; an application filed January 17, 1997 having Serial No. 08/785,353 and entitled "METHOD FOR SORTING INTEGRATED CIRCUIT ~~DEVICES",~~ DEVICES," now U.S. Patent 5,927,512, issued July 27, 1999; an application filed February 17, 1997 having Serial No. 08/801,565 and entitled "METHOD OF SORTING A GROUP OF INTEGRATED CIRCUIT DEVICES FOR THOSE DEVICES REQUIRING SPECIAL ~~TESTING",now~~ TESTING," now U.S. Patent 5,844,803, issued December 1, 1998; an application filed February 26, 1997 having Serial No. 08/806,442 and entitled "METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND RE-DIRECTING ~~IC'S MIS-PROCESSED~~ ICS MIS-PROCESSED DURING THEIR ~~MANUFACTURE",~~ MANUFACTURE," now U.S. Patent 5,915,231, issued June 22, 1999; and an application filed March 24, 1997 having Serial No. 08/822,731 and entitled "METHOD FOR CONTINUOUS, NON LOT-BASED INTEGRATED CIRCUIT ~~MANUFACTURING",~~ MANUFACTURING," now U.S. Patent 5,856,923, issued January 5, 1999.

Please amend paragraph **[0003]** as follows:

[0003] Field of the Invention: The present invention relates in general to integrated circuit semiconductor device (IC) manufacturing. More specifically, it relates to methods in IC

manufacturing processes for using data regarding manufacturing procedures ~~IC's~~ ICs have undergone, such as repair procedures, to select procedures the ~~IC's~~ ICs will undergo, such as additional repair procedures.

Please amend paragraph **[0004]** as follows:

[0004] State of the Art: As shown in FIG. 1, a typical process 10 for manufacturing very small electronic semiconductor device circuits referred to as "Integrated Circuits" ~~(IC's)~~ (ICs) begins with the ~~IC's~~ ICs being formed or "fabricated" on the surface of a wafer 12 of semiconductor material, such as silicon. Once fabricated, ~~IC's~~ ICs are electronically probed to determine whether they are functional (i.e., "good") or nonfunctional (i.e., "bad"). If any ~~IC's~~ ICs are found to be bad, an attempt is made to repair those ~~IC's~~ ICs by replacing nonfunctional circuit elements in the ~~IC's~~ ICs with spare circuit elements. For example, Dynamic Random Access Memory (DRAM) ~~IC's~~ ICs are typically repaired by replacing nonfunctional rows or columns of memory cells in the ~~IC's~~ ICs with spare rows or columns.

Please amend paragraph **[0005]** as follows:

[0005] These repairs are not always successful, because the number of spare circuit elements on an IC may be exhausted before all nonfunctional circuit elements on the IC are replaced, and because some circuit elements on ~~IC's~~ ICs have no spares to replace them. As a result, a number of bad ~~IC's~~ ICs typically remain on a wafer 12 even after attempts are made to repair the ~~IC's.~~ ICs. The location of bad ~~IC's~~ ICs on a wafer 12, along with the location of any good ~~IC's~~ ICs on the wafer 12, is typically stored in a computer database commonly referred to as a "wafer map."

Please amend paragraph **[0006]** as follows:

[0006] After being probed and, if necessary, repaired, ~~IC's~~ ICs begin an assembly process with their wafer 12 being mounted on an adhesive film. In some instances, the film is a special high-adhesion Ultraviolet (U.V.) film. Without cutting the adhesive film, ~~IC's~~ ICs are

sawed from their wafer 12 into discrete IC dice or "chips" using high-speed precision dicing equipment. IC dice mounted on U.V. film are then exposed to U.V. light to loosen the grip of the film on the dice. IC dice identified as good by their wafer map are then each "picked" by automated equipment from their sawed wafer 12 and its associated film and "placed" on an epoxy-coated bonding site of one lead frame in a strip of interconnected lead frames, while IC dice identified as bad are discarded into a scrap bin 14. The epoxy attaching the good IC dice to their lead frames is then cured, and the attached dice are wire bonded to their lead frames using high-speed bonding equipment.

Please amend paragraph **[0008]** as follows:

[0008] After assembly, discrete IC devices are tested in a simple electronic test referred to as an "opens/shorts" test, which checks for "opens" (i.e., no connection) within the devices where connections should exist and "shorts" (i.e., a connection) where connections should not exist. Devices that pass the opens/shorts test proceed on through the process 10 to various ~~burn-in~~ burn-in and test procedures where they are tested for functionality, operability, and reliability, and devices that pass these burn-in and test procedures are then typically shipped to customers.

Please amend paragraph **[0011]** as follows:

[0011] Similarly, as shown in FIG. 2, a typical process 20 for manufacturing so-called "flip-chip" and "Chip-On-Board" (COB) Multi-Chip Modules ~~(MCM's),~~ (MCMs), in which multiple IC dice are typically attached directly to a substrate, such as a printed circuit board (PCB), begins with ~~IC's~~ ICs being fabricated on the surface of a semiconductor wafer 22 in the same manner as described above. Once fabricated, ~~IC's~~ ICs are electronically probed to determine whether they are good or bad, and if any ~~IC's~~ ICs are found to be bad, an attempt is made to repair those ~~IC's~~ ICs (i.e., make them good ~~IC's)~~ ICs) by replacing nonfunctional circuit elements in the ~~IC's~~ ICs with spare circuit elements. The locations of good and bad ~~IC's~~ ICs on a wafer 22 are then typically stored in an electronic wafer map.

Please amend paragraph **[0012]** as follows:

[0012] After being probed and, if necessary, repaired, ~~IC's~~ ICs begin an assembly process with their wafer 22 being mounted on an adhesive film. Without cutting this film, ~~IC's~~ ICs are then sawed from their wafer 22 into discrete IC dice using high-speed precision dicing equipment. IC dice that are mounted on the special high-adhesion U.V. film described above are then exposed to U.V. light to loosen the grip of the film on the dice.

Please amend paragraph **[0013]** as follows:

[0013] IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer 22 and its associated film, typically for attachment to a substrate in a panel of multiple substrates, such as a panel of interconnected ~~PCB's.~~ PCBs. If the assembly process is a flip-chip process, picked dice are then flipped and directly attached at their active, ~~frontside~~ front side surfaces to substrates to form ~~MCM's.~~ MCMs. If the assembly process is a COB process, picked dice are directly attached at their inactive, ~~backside~~ back side surfaces to adhesive-coated bonding sites of substrates to form ~~MCM's.~~ MCMs. IC dice identified as bad are discarded into a scrap bin 24.

Please amend paragraph **[0014]** as follows:

[0014] Panels of ~~MCM's~~ MCMs are then cured. If the assembly process is a COB process, the ~~MCM's~~ MCMs may be plasma cleaned, if necessary, and the COB IC dice are then wire bonded to their substrates using high-speed bonding equipment.

Please amend paragraph **[0015]** as follows:

[0015] After assembly, panels of ~~MCM's~~ MCMs are tested in an opens/shorts test. Panels having COB IC dice that pass the opens/shorts test proceed on through the manufacturing process 20 so the dice can be encapsulated using an overmold, hard cover, or so-called "glob" top, while panels having flip-chip IC dice that pass the opens/shorts test may have their dice encapsulated using an underfill followed by an overmold, hard cover, or glob top. As will be

described in more detail below, alternatively, flip-chip IC dice may be encapsulated after burn-in and test procedures. The disposition of panels of ~~MCM's~~ MCMs having COB and flip-chip attached IC dice that fail the opens/shorts test will be described in more detail below.

Please amend paragraph **[0016]** as follows:

[0016] Panels of ~~MCM's~~ MCMs having both COB and flip-chip IC dice, including those panels having flip-chip IC dice that were not encapsulated, are then singulated into discrete ~~MCM's,~~ MCMs, typically by a shear press or router. After singulation, those ~~MCM's~~ MCMs having encapsulated IC dice have their dice tested again in an additional opens/shorts test to check for problems caused by the encapsulation. ~~MCM's~~ MCMs having encapsulated dice that pass this additional opens/shorts test, as well as ~~MCM's~~ MCMs having dice that were not encapsulated, then proceed on in the manufacturing process 20 to various burn-in and test procedures. The disposition of any ~~MCM's~~ MCMs having encapsulated dice that fail the additional opens/shorts test will be described in more detail below.

Please amend paragraph **[0017]** as follows:

[0017] After the burn-in and test procedures, ~~MCM's~~ MCMs having unencapsulated flip-chip IC dice that pass the procedures proceed on in the process 20 so their dice may be covered with an overmold, hardcover, or glob top. Dice covered in this manner are then checked in a further opens/shorts test for problems caused by their being covered, and ~~MCM's~~ MCMs having dice that pass this further test are then typically shipped to customers. ~~MCM's~~ MCMs having encapsulated IC dice that pass the burn-in and test procedures skip this final opens/shorts test and typically proceed to shipping.

Please amend paragraph **[0018]** as follows:

[0018] ~~MCM's~~ MCMs having attached IC dice that fail any of the opens/shorts, burn-in, and test procedures are checked to determine whether their associated IC dice are repairable. This "check" typically includes an electronic querying of the IC dice to determine

whether enough spare circuit elements remain in the dice for effecting repairs. ~~MCM's~~ MCMs determined to have unrepairable IC dice are then either reworked using replacement IC dice in an expensive and time-consuming procedure or scrapped in a scrap bin 26, while ~~MCM's~~ MCMs having IC dice that are repairable are repaired, typically by replacing nonfunctional circuit elements in the IC dice with spare circuit elements. After being repaired, these ~~MCM's~~ MCMs then reenter the manufacturing process 20 just prior to the opens/shorts, burn-in, or test procedures they failed.

Please amend paragraph **[0019]** as follows:

[0019] As discussed above, electronic querying of IC dice to determine whether spare circuit elements are available to effect repairs increases the time required to move ~~MCM's~~ MCMs through the manufacturing process 20 and places an additional burden on expensive testing resources. Also, IC dice that require repair, and are found to be unrepairable only after the assembly process, waste assembly time, materials, and resources and necessitate the scrapping or reworking of ~~MCM's~~ MCMs that may contain many functional dice. It is desirable, then, to have an IC manufacturing method for identifying unrepairable IC dice so they may be kept out of COB, ~~flip-chip,~~ flip-chip and other MCM assembly processes.

Please amend paragraph **[0020]** as follows:

[0020] As described in U.S. Patent ~~No.'s~~ Nos. 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify IC dice. Such methods take place "off" the manufacturing line, and involve the use of electrically retrievable identification (ID) codes, such as so-called "fuse ~~ID's,"~~ IDs," programmed into individual IC dice to identify the dice. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses or ~~anti-fuses~~ anti-fuses in an IC die using electric current or a laser so that when the fuses or anti-fuses are accessed, they output a preprogrammed ID code. Unfortunately, none of these methods addresses the problem of identifying unrepairable IC dice "on" a manufacturing line.

Please amend paragraph **[0021]** as follows:

[0021] The present invention provides a method in an integrated circuit (IC) manufacturing process for using data regarding manufacturing procedures ~~IC's~~ ICs have undergone, such as repair procedures at probe, to select manufacturing procedures the ~~IC's~~ ICs will undergo, such as additional repair procedures during back-end testing. The ~~IC's~~ ICs are each programmed with a substantially unique identification (ID) code, such as a fuse ID.

Please amend paragraph **[0022]** as follows:

[0022] The method includes storing data in association with the ID codes of the ~~IC's~~ ICs that identifies manufacturing procedures the ~~IC's~~ ICs have undergone. This data may identify spare circuitry already used to repair the ~~IC's~~ ICs at probe, for example, or spare circuitry available to repair the ~~IC's.~~ ICs. The ID codes of the ~~IC's~~ ICs are automatically read, for example, at an opens/shorts test during the manufacturing process. The data stored in association with the ID codes is then accessed, and manufacturing procedures the ~~IC's~~ ICs will undergo, such as additional repair procedures during back-end testing, are selected in accordance with the accessed data. Thus, for example, the accessed data may indicate that insufficient spare circuitry is available on an IC to effect repairs, so the IC can proceed directly to a scrap bin without being "queried" to determine the availability of spare circuitry, as is traditionally necessary. The present invention thus eliminates the time-wasting conventional process of querying ~~IC's~~ ICs prior to repair or scrapping.

Please amend paragraph **[0023]** as follows:

[0023] Further embodiments include methods of manufacturing IC devices and ~~Multi-Chip~~ Multi-Chip Modules ~~(MCM's)~~ (MCMs) which incorporate the method described above.

Please amend paragraph **[0024]** as follows:

[0024] In an additional embodiment, a method in an MCM manufacturing process for diverting good but unrepairable IC dice from the process includes storing data in association with

ID codes, such as fuse ~~ID's,~~ IDs, of the ~~IC's~~ ICs that identifies ~~IC's~~ ICs that are a) good and repairable, b) good but unrepairable, and c) bad. In the inventive method, the ID codes of the ~~IC's~~ ICs are automatically read, and the data stored in association with the ID codes is accessed. ~~IC's~~ ICs identified as good but unrepairable by the accessed data are diverted to other IC manufacturing processes, while ~~IC's~~ ICs identified as bad are discarded, and ~~IC's~~ ICs identified as good and repairable are assembled into ~~MCM's.~~ MCMs.

Please amend paragraph **[0025]** as follows:

[0025] The present invention thus prevents ~~IC's~~ ICs that are unrepairable from being assembled into ~~MCM's,~~ MCMs, such as Single In-Line Memory Modules ~~(SIMM's),~~ (SIMMs), and thus prevents the reworking or scrapping of ~~MCM's~~ MCMs into which unrepairable ~~IC's~~ ICs have been assembled.

Please amend paragraph **[0032]** as follows:

[0032] As shown in FIG. 3A, an inventive process 30 for manufacturing Dynamic Random Access Memory (DRAM) Integrated Circuit semiconductor devices ~~(IC's)~~ (ICs) begins with DRAM ~~IC's~~ ICs being fabricated in a fabrication step 32 on the surface of a semiconductor wafer 34. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including Static Random Access Memory (SRAM) ~~IC's,~~ ICs, Synchronous DRAM (SDRAM) ~~IC's,~~ ICs, processor ~~IC's,~~ ICs, Single In-line Memory Modules ~~(SIMM's),~~ (SIMMs), Dual In-line Memory Modules ~~(DIMM's),~~ (DIMMs), Rambus In-Line Memory Modules (RIMM), Small Outline Rambus In-Line Memory Modules (SO-RIMM), Personal Computer Memory Format (PCMCIA), Board-Over-Chip type substrate configurations, and other Multi-Chip Modules ~~(MCM's).~~ (MCMs). It will also be understood that although the present invention will be described below in the context of a wire bond/lead frame assembly process, either a conventional lead frame or leads-over-chip configuration using adhesive tape on the lead frame or the semiconductor die or non-conductive adhesive on the active surface of the semiconductor die (LOC), the present invention is applicable to any IC

assembly process, including, for example, Chip On Board (COB)-either single semiconductor device or the modular form of multiple semiconductor device ~~IC's,~~ ICs, Board Over Chip (BOC)-either single semiconductor device or the modular form of multiple semiconductor device ~~IC's,~~ ICs, any configuration of substrate and component including Tessera style electrical components (film on elastomer), flip-chip processes (as will be described below with respect to ~~FIG.'s~~ FIGS. 4A and 4B), Tape-Automated Bonding (TAB) processes, and wafer scale semiconductor device packages or packaging, either the entire wafer as a whole, multiple semiconductor devices as portions of the wafer which are singulated and packaged, or the singulation of the semiconductor devices on the wafer which are later packaged and/or mounted.

Please amend paragraph **[0033]** as follows:

[0033] Once fabricated, the DRAM ~~IC's~~ ICs are electronically probed in a probe step 36 to determine whether they are good or bad, and if any DRAM ~~IC's~~ ICs are found to be bad, an attempt is made to repair those ~~IC's~~ ICs by replacing nonfunctional rows or columns in the ~~IC's~~ ICs with spare rows or columns. The location of bad DRAM ~~IC's~~ ICs on a wafer 34, along with the location of any good DRAM ~~IC's~~ ICs on the wafer 34, is stored in a computer in an electronic wafer map in association with data identifying spare rows and columns still available in each of the DRAM ~~IC's~~ ICs after any repairs performed at the probe step 36. Of course, it will be understood that the stored data may alternatively identify spare rows and columns used in each of the DRAM ~~IC's~~ ICs to effect repairs at the probe step 36.

Please amend paragraph **[0034]** as follows:

[0034] During the probe step 36, DRAM ~~IC's~~ ICs fabricated on the wafers 34 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each DRAM IC is then stored in association with the repair data 38 for that IC. The fuse ID may identify, for example, a wafer lot ID, the week the DRAM ~~IC's~~ ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. As a result of storing the fuse ID for each DRAM IC in association with the repair data 38, the availability of

spare rows or columns for effecting post-probe repairs in a particular DRAM IC can be determined by using the fuse ID of the IC to access the stored repair data 38 for the IC, as will be described in more detail below.

Please amend paragraph **[0035]** as follows:

[0035] It will be understood, of course, that the present invention includes within its scope DRAM ~~IC's~~ ICs and other ~~IC's~~ ICs having any ID code, such as a dot code, bar code, or any suitable type marking code on the ~~IC's,~~ ICs, including those having fuse ~~ID's.~~ IDs. It will also be understood that the ~~IC's~~ ICs may be programmed with their fuse ~~ID's~~ IDs at steps in the manufacturing process 30 other than the probe step 36.

Please amend paragraph **[0036]** as follows:

[0036] After being probed and, if necessary, repaired, DRAM ~~IC's~~ ICs enter an assembly process 40 in which good ~~IC's~~ ICs are assembled into IC devices, as will be described in more detail below with respect to FIG. 3B, while bad ~~IC's~~ ICs are discarded in a scrap bin 42. In addition, DRAM ~~IC's~~ ICs 44 that have been diverted from COB and flip-chip manufacturing process flows enter the assembly process 40 and are also assembled into IC devices. The DRAM ~~IC's~~ ICs 44 are diverted from the COB and flip-chip process flows because so many of their spare rows and columns have been used at probe to effect repairs in the DRAM ~~IC's~~ ICs 44 that the DRAM ~~IC's~~ ICs 44 fall below a minimum threshold level of repairability, as will be described in more detail below with respect to ~~FIG.'s~~ FIGS. 4A and 4B.

Please amend paragraph **[0037]** as follows:

[0037] After the assembly process 40, discrete DRAM IC devices are tested in an opens/shorts test 46. There, the fuse ID of the DRAM IC in each IC device is automatically read and correlated with the repair data 38 produced in the manufacturing process 30 or repair data 48 produced in a COB or flip-chip process flow as described below. It should be understood that although the fuse ~~ID's~~ IDs of DRAM ~~IC's~~ ICs in the process 30 are typically read electronically,

they may also be read optically if the fuse ~~ID's~~ IDs consist of "blown" laser fuses that are optically accessible. It should also be understood that the fuse ~~ID's~~ IDs of DRAM ~~IC's~~ ICs may be read at steps in the process 30 other than the opens/shorts test 46.

Please amend paragraph **[0040]** as follows:

[0040] It should be understood, of course, that the present invention is applicable to situations in a wide variety of IC manufacturing processes in which data regarding manufacturing procedures the ~~IC's~~ ICs have undergone, such as repair procedures at probe, may be accessed through the use of fuse ~~ID's~~ IDs and other ID codes to determine procedures the ~~IC's~~ ICs should undergo, such as post-probe repairs.

Please amend paragraph **[0041]** as follows:

[0041] As stated above, the assembly process 40 of FIG. 3A is shown in more detail in FIG. 3B. In the process 40, probed and repaired semiconductor wafers enter a wafer saw step 60 and are mounted on an adhesive film. The film may be any one of a wide variety of adhesive films used for this purpose, including, for example, a special high-adhesion U.V. film. Without cutting the film, DRAM ~~IC's~~ ICs are then sawed from their wafer into discrete IC dice using ~~high speed~~ high-speed precision dicing equipment. DRAM IC dice that are mounted on the special high-adhesion U.V. film are then exposed to U.V. light in an optional U.V. exposure step 62 to loosen the grip of the film on the dice.

Please amend paragraph **[0042]** as follows:

[0042] DRAM IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer and its associated film in a die attach step 64 and placed on an epoxy-coated bonding site of one lead frame in a strip of interconnected lead frames, while DRAM IC dice identified as bad are discarded into the scrap bin 42. In addition, DRAM ~~IC's~~ ICs 44 that have been diverted from COB and flip-chip manufacturing process flows enter the assembly process 40 and are also placed on an adhesive-coated bonding

site of one lead frame in a lead frame strip. These diverted DRAM ~~IC's~~ ICs 44 will be described in more detail below with respect to ~~FIG.'s~~ FIGS. 4A and 4B. The adhesive attaching the good DRAM IC dice to their lead frames is then cured, if required, in a cure step 66, and the attached dice are wire bonded to their lead frames using high-speed bonding equipment in a wire bond step 68.

Please amend paragraph **[0043]** as follows:

[0043] Once wire bonded, DRAM IC dice and their lead frames continue the assembly process 40 by being formed into DRAM IC packages using a hot thermosetting plastic encapsulant injected into a mold in an overmold step 70. DRAM IC packages are then cured in a further cure step 72 to set their plastic encapsulant. After encapsulation and curing, leads of the lead frames projecting from the packages may be dipped in a cleansing chemical bath in a ~~de-flash~~ de-flash process 74 and then may be electroplated with a lead/tin finish if they are not already plated. Finally, connections between the lead frames of different DRAM IC packages are then cut in a singulate step 76 to separate the packages into discrete DRAM IC devices.

Please amend paragraph **[0044]** as follows:

[0044] In another embodiment of the present invention shown in FIG. 4A, an inventive COB or flip-chip process 80 for manufacturing DRAM ~~SIMM's~~ SIMMs begins with DRAM ~~IC's~~ ICs being fabricated in a fabrication step 82 on the surface of a semiconductor wafer 84. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including SRAM ~~IC's,~~ ICs, SDRAM ~~IC's,~~ ICs, processor ~~IC's,~~ ICs, and modules using such IC devices, such as ~~DIMM's, RIMM's, SO-RIMM'S, PCMCIA's, COB's, BOC's,~~ DIMMs, RIMMs, SO-RIMMS, PCMCIAs, COBs, BOCs, and other ~~MCM's.~~ MCMs. It will also be understood that although the present invention will be described below in the context of both a COB process and a flip-chip assembly process, the present invention is applicable to any IC assembly process, including, for example, Tape-Automated Bonding (TAB) processes, wafer scale processes including packaging, partial wafer scale processes including

packaging, etc. It should be further understood that the present invention relates to any type IC that has been singulated by any type singulation process or apparatus, such as wafer saw singulation, laser apparatus singulation, laser/water apparatus singulation (cool laser singulation), water jet apparatus singulation, etc.

Please amend paragraph **[0045]** as follows:

[0045] Once fabricated, the DRAM ~~IC's~~ ICs are electronically probed in a probe step 86 to determine whether they are good or bad, and if any DRAM ~~IC's~~ ICs are found to be bad, an attempt is made to repair the ~~IC's~~ ICs by replacing nonfunctional rows or columns in the ~~IC's~~ ICs with spare rows or columns. The locations of bad DRAM ~~IC's~~ ICs on a wafer 84, along with the locations of any good DRAM ~~IC's~~ ICs on the wafer 84, are stored in a computer in an electronic wafer map in association with repair data 48 identifying spare rows and columns still available in each of the DRAM ~~IC's~~ ICs after any repairs performed at the probe step 86.

Please amend paragraph **[0046]** as follows:

[0046] During the probe step 86, DRAM ~~IC's~~ ICs fabricated on the wafers 84 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each DRAM IC is then stored in association with the repair data 48 for that IC. The fuse ID may identify, for example, a wafer lot ID, the week the DRAM ~~IC's~~ ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

Please amend paragraph **[0047]** as follows:

[0047] It will be understood, of course, that the present invention includes within its scope ~~IC's~~ ICs having any ID code, including those having fuse ~~ID's.~~ IDs. It will also be understood that the ~~IC's~~ ICs may be programmed with their fuse ~~ID's~~ IDs at steps in the manufacturing process 80 other than the probe step 86.

Please amend paragraph **[0048]** as follows:

[0048] After being probed and, if necessary, repaired, DRAM ~~IC's~~ ICs enter an assembly process 90 in which good ~~IC's~~ ICs are assembled into panels of physically interconnected DRAM ~~SIMM's,~~ SIMMs, as will be described in more detail below with respect to FIG. 4B, while bad ~~IC's~~ ICs are discarded in a scrap bin 92. In addition, DRAM ~~IC's~~ ICs 44 in which so many spare rows and columns have been used at the probe step 86 to effect repairs that the ~~IC's~~ ICs 44 fall below a minimum threshold of repairability are diverted from the COB or flip-chip process 80 for use in the standard assembly process 40 of ~~FIG.'s~~ FIGS. 3A and 3B. Although a "minimum threshold of repairability" can be set at any level, it might be set, for example, at a level at which statistically the available spare rows and columns in a DRAM IC would only be able to effect repairs in an unacceptably low percentage (e.g., 50%) of cases of failures. Thus, the diverted DRAM ~~IC's~~ ICs 44 typically include those ~~IC's~~ ICs that have exhausted their spare rows and columns in repairs at the probe step 86 and those ~~IC's~~ ICs that have some, but not enough, spare rows and columns left after being repaired at the probe step 86.

Please amend paragraph **[0049]** as follows:

[0049] The present invention thus prevents DRAM ~~IC's~~ ICs that would be repairable in few or none of the possible cases of failure from being assembled into DRAM ~~SIMM's~~ SIMMs and other ~~MCM's,~~ MCMs, and thus prevents the waste of time and resources associated with scrapping or reworking ~~MCM's~~ MCMs into which such ~~IC's~~ ICs have traditionally been assembled.

Please amend paragraph **[0050]** as follows:

[0050] After the assembly process 90, panels of DRAM ~~SIMM's~~ SIMMs are tested in an opens/shorts test 96. There, the fuse ID of each DRAM IC in each DRAM SIMM is automatically read and correlated with the repair data 48. It should be understood that although the fuse ~~ID's~~ IDs of DRAM ~~IC's~~ ICs in the process 80 are typically read electronically, they may also be read optically if the fuse ~~ID's~~ IDs consist of "blown" laser fuses that are optically

accessible. It should also be understood that the fuse ~~ID's~~ IDs of DRAM ~~IC's~~ ICs may be read at steps in the process 80 other than the opens/shorts test 96.

Please amend paragraph **[0051]** as follows:

[0051] When the manufacturing process 80 is a COB process, panels of DRAM ~~SIMM's~~ SIMMs having COB IC dice that pass the opens/shorts test 96 proceed to an encapsulation step 98 so the dice can be encapsulated using an overmold, hard cover, or glob top. Alternatively, when the manufacturing process 80 is a flip-chip process, panels of DRAM ~~SIMM's~~ SIMMs having flip-chip IC dice that pass the opens/shorts test 96 may have their dice encapsulated at the encapsulation step 98 using an underfill followed by an overmold, hard cover, or glob top. As will be described in more detail below, alternatively, the flip-chip IC dice may be encapsulated after burn-in and test procedures. The disposition of panels of DRAM ~~SIMM's~~ SIMMs having IC dice that fail the opens/shorts test will be described in more detail below.

Please amend paragraph **[0052]** as follows:

[0052] Panels of DRAM ~~SIMM's~~ SIMMs having either COB or flip-chip IC dice, including those panels of ~~SIMM's~~ SIMMs having flip-chip IC dice that were not encapsulated at the encapsulation step 98, are then singulated into discrete DRAM ~~SIMM's~~ SIMMs at a singulation step 100 by, for example, a water jet or a shear press. This singulation step 100 may, for example, divide a "ten" panel of ten physically attached DRAM ~~SIMM's~~ SIMMs into ten discrete DRAM ~~SIMM's.~~ SIMMs.

Please amend paragraph **[0053]** as follows:

[0053] After singulation, DRAM ~~SIMM's~~ SIMMs having encapsulated IC dice are tested again in an additional opens/shorts test 102 to check for problems caused by the encapsulation step 98. DRAM ~~SIMM's~~ SIMMs having encapsulated dice that pass this additional opens/shorts test 102, as well as DRAM ~~SIMM's~~ SIMMs having dice that were not encapsulated, then proceed on in the manufacturing process 80 to burn-in testing 104 and

back-end testing 106. The disposition of those DRAM ~~SIMM's~~ SIMMs having encapsulated IC dice that fail the additional opens/shorts test 102 will be described in more detail below. The fuse ~~ID's~~ IDs of the IC dice in the DRAM ~~SIMM's~~ SIMMs may also be automatically read at this additional opens/shorts test 102.

Please amend paragraph **[0054]** as follows:

[0054] After the burn-in and test procedures 104 and 106, DRAM ~~SIMM's~~ SIMMs having ~~un-encapsulated~~ unencapsulated flip-chip IC dice that pass the procedures 104 and 106 proceed on in the process 80 to an optional cover step 108 so their dice may be covered with an overmold, hardcover, or glob top. Dice covered in this manner are then checked in a further opens/shorts test 108 for problems caused by their being covered, and DRAM ~~SIMM's~~ SIMMs having dice that pass this further test are then typically shipped in a shipping step 110 to customers. DRAM ~~SIMM's~~ SIMMs having encapsulated IC dice that pass the burn-in and test procedures 104 and 106 skip this covering and final opens/shorts test step 108 and proceed to the shipping step 110. Of course, the fuse ~~ID's~~ IDs of the IC dice in the DRAM ~~SIMM's~~ SIMMs tested at any of the burn-in, back-end test, and opens/shorts test procedures 104, 106, and 108 may be automatically read at any one or all of those tests.

Please amend paragraph **[0055]** as follows:

[0055] DRAM ~~SIMM's~~ SIMMs having IC dice that fail any of the opens/shorts, burn-in, and test procedures 96, 102, 104, 106 and 108 proceed to repair 112. Those DRAM ~~SIMM's~~ SIMMs having DRAM IC dice that do not have enough available spare rows and columns to effect repairs, and thus are unrepairable, are identified as such when their repair data 48 is accessed at any one of the opens/shorts, burn-in, and back-end tests 96, 102, 104, 106, and 108, and these ~~SIMM's~~ SIMMs proceed directly to rework (described below) or a scrap bin 114 without the need to query them. Of course, DRAM ~~SIMM's~~ SIMMs having DRAM IC dice identified by their repair data 48 as being repairable are repaired, typically by replacing nonfunctional rows and columns with spare rows and columns in the same manner as described

above. After being repaired, these DRAM ~~SIMM's~~ SIMMs then reenter the manufacturing process 80 just prior to the opens/shorts, burn-in, or test procedures 96, 102, 104, 106 or 108 they failed.

Please amend paragraph **[0056]** as follows:

[0056] Those DRAM ~~SIMM's~~ SIMMs that are reworkable by replacing one or more ~~non-functioning~~ non-functioning IC dice proceed through a Known Good Die (KGD) process in which a DRAM KGD (*i.e.*, a burned-in, fully tested, fully functional DRAM) replaces the non-functioning IC dice on the ~~SIMM's~~ SIMMs in a replacement step 116. The KGD repairs are then tested in a repair step 118, and if the repairs are successful, the repaired DRAM ~~SIMM's~~ SIMMs reenter the manufacturing process 80 just prior to the back-end test procedures 106. If the repairs are not successful, the DRAM ~~SIMM's~~ SIMMs may return to the repair step 112 to be reworked again or, if they are not reworkable, to be scrapped in the scrap bin 114.

Please amend paragraph **[0057]** as follows:

[0057] As stated above, the assembly process 90 of FIG. 4A is shown in more detail in FIG. 4B. In the process 90, probed and repaired semiconductor wafers enter a wafer saw step 120 and are mounted on an adhesive film. The film may be any one of a wide variety of adhesive films used for this purpose, including, for example, a special high-adhesion U.V. film. Without cutting the film, DRAM ~~IC's~~ ICs are then sawed from their wafer into discrete DRAM IC dice using high-speed precision dicing equipment. DRAM IC dice that are mounted on the special high-adhesion U.V. film are then exposed to U.V. light in an optional U.V. exposure step 122 to loosen the grip of the film on the dice.

Please amend paragraph **[0058]** as follows:

[0058] IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer and its associated film at an attachment step 124. If the assembly process 90 is a flip-chip process, multiple picked dice are then flipped and

directly attached at their active, ~~frontside~~ front side surfaces to a panel of ~~PCB's~~ PCBs or other substrates to form, for example, DRAM ~~SIMM's.~~ SIMMs. If the assembly process 90 is a COB process, multiple picked dice are directly attached at their inactive, ~~backside~~ back side surfaces to an adhesive-coated bonding site of a panel of ~~PCB's~~ PCBs or other substrates to form, for example, DRAM ~~SIMM's.~~ SIMMs. DRAM ~~IC's~~ ICs identified as bad are discarded into the scrap bin 92, while DRAM ~~IC's~~ ICs 44 that have used so many of their spare rows and columns in repairs at the probe step 86 that they fall below the minimum threshold of repairability are diverted to the standard assembly process 40 of ~~FIG.'s~~ FIGS. 3A and 3B. Panels of DRAM ~~SIMM's~~ SIMMs are then cured at a cure step 126. If the assembly process 90 is a COB process, the panels may be plasma cleaned in an optional plasma cleaning step 128, if necessary, and the COB IC dice are then wire bonded at a wire bond step 130 to their DRAM ~~SIMM's~~ SIMMs using high-speed bonding equipment. DRAM ~~SIMM's~~ SIMMs then proceed to the opens/shorts test 96 described above with respect to FIG. 4A.